Docket No. 034299-336

## REMARKS

In a communication from the Patent Office, mailed August 09, 2002, the examiner imposed a restriction requirement requiring election between claims 1-11, drawn to a semiconductor device (class 257, subclass 347) and claims 12-24 (class 438, subclass +1). In response to the restriction requirement, Applicant elected claims 1-11 and reserved the right to file claims 12-24 in a divisional patent application.

On December 16, 2002, the examiner called the undersigned to inform that claims 1-11 required either amendment or an election from among various species. Applicant proposed the amendments set forth in this Preliminary Amendment to avoid further election. Accordingly, entry of this Preliminary Amendment is requested prior to examination of the subject divisional patent application. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 408-282-1857.

Respectfully submitted,

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## **VERSION WITH MARKINGS TO SHOW CHANGES MADE**

- 1. (Once Amended) A semi[-]conductor device eomprising formed in an integrated way on a substrate, comprising:
- [-] a first dynamic threshold voltage MOS transistor (10) with having a gate (116), and a channel (111) of a first conductivity type; and:

a first doped zone of the first conductivity type coupled to the channel of said first MOS transistor; and

[-] a current limiter [means] (20, 30) connected coupled between the gate and the channel of said first MOS transistor and said first doped zone, said current limiter comprising

characterised in that this first MOS transister is fitted with a first-doped zone (160) of the first conductivity type, connected to the channel, and in that the current limiter means comprises a second doped zone (124, 124a) of a second conductivity type, placed against the first doped zone and electrically connected to the first doped zone by an in ohmic contact with said first doped zone connection path (180).

2. (Once Amended) AThe device according to claim 1, wherein the current limiter means is comprises a second MOS transistor—(20), the second doped zone—(124) embodying the source and a third doped zone (122) of the same conductivity type as the second doped zone forming the source and drain of said second transistor.

- 3. (Once Amended) AThe device according to claim 2, wherein the second transistor includes a gate (126) connected to a gate polariszation terminal (127).
- 4. (Once Amended) A<u>The</u> device according to claim 2, wherein the second transistor—(20) has a gate (126) connected coupled to said second doped zone—(124).
- 5. (Once Amended) AThe device according to claim 4, including further comprising a terminal (128) that is coupled to in contact with the gate (126) of said second transistor and towith the second doped zone (124).
- 6. (Once Amended) AThe device according to claim 4, wherein a drain of said second transistor the third deped area (122) is connected coupled to the gate (116) of the first MOS transistor (10).
- 7. (Once Amended) AThe device according to claim 1, wherein the current limitering means is comprises a diode (30), the second doped zone (124a) embodying a first terminal of the diode and a third doped zone (122a), of a conductivity type opposite to that of the conductivity type of the second doped zone, forming embodying a second terminal of the diode terminals.
- 8. (Once Amended) AThe device according to claim 7, including further comprising a fourth doped zone (121), placed disposed between the second and third doped zones, said fourth doped zone having the same conductivity type as one of the

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conductivity type of either the second andor third zones, with a doping concentration lower than that of that zone.

- 9. (Once Amended) AThe device according to claim 7, wherein the third doped zone (122a) is connected coupled to the gate of the first MOS transistor.
- (Once Amended) AThe device according to claim 8, wherein the diode 10. comprises a gate (126) extending over the fourth doped zone (121).
- (Once Amended) AThe device according to claim 10, wherein said diode 11. gate (126) is connected coupled to one of the diode terminals (122a, 124a).